UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,473	01/13/2006	Masaki Murase	SON-3058	9263

23353 7590 03/30/2010

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
03/30/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/564,473
Filing Date: January 13, 2006
Appellant(s): MURASE ET AL.

Christopher M. Tobin
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/12/2010 appealing from the Office action mailed 08/20/2009.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20060164364	**Murase**	**7-2006**
JP 2002-009594	**Iemoto**	**1-2002**
6,897,909	**Ochiai**	**8-2002**
JP 10-177368	**Chin**	**6-1998**

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 7-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of JP Iemoto Hiroshi (2000-191367) hereinafter, Iemoto.

4. In regards to claim 7, AAPA teaches a display device comprising:

a level shifter (fig. 1 (1)) configured to change an amplitude of gradation data from a first voltage range to a second voltage range (fig. 2 (b) and (c)), amplified gradation data being said gradation data at said second voltage range [0009-0010],

output data during a period other than said quiescent period being said amplified gradation data (fig. 2 (c)).

AAPA fails to teach wherein output data during a quiescent period is dummy data.

However, Iemoto teaches wherein output data during a quiescent period is dummy data (Abstract, (0008—0012, 0082-0084]).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the dummy data during a quiescent period as taught by Iemoto in order to reduce fluctuations in the operating frequency of the circuit as stated in the abstract of Iemoto

5. In regards to claim 8, AAPA teaches the display device according to claim 7, wherein a maximum value of said first voltage range is lower than a maximum value of

said second voltage range (fig. 2 A-C).

6. In regard to claim 9, AAPA teaches the display device according to claim 7, wherein said first voltage range is 0 volts to 3 volts and said second voltage range is 0 volts to 6 volts (fig. 2 B-C).

7. In regards to claim 10, AAPA teaches the display device according to claim 7, wherein said quiescent period is during which said gradation data is held at a constant logical level for a constant period at a constant cycle (fig. 2 (B-C) T2).

8. In regards to claim 11, AAPA as modified by Iemoto teaches the display device according to claim 10, wherein said dummy data has a logical level opposite to said constant logical level (Abstract, (0008—0012, 0082-0084] Iemoto) .

9. In regards to claim 12, AAPA does not disclose expressly wherein said quiescent period is a horizontal blanking period.

However, Applicant has not disclosed that having wherein said quiescent period is a horizontal blanking period instead of a vertical blanking period [0010] provides an advantage, is used for a particular purpose, or solves a stated problem. As such, having quiescent period is a horizontal blanking period is an obvious matter of design choice.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have quiescent period is a horizontal blanking period because either configuration would perform equally well at providing the predictable result of providing dummy data during a blanking period to avoid various influences due to the variation in delay time and provide for a desirable display.

10. In regards to claim 13, AAPA teaches the display device according to claim 10, wherein said quiescent period is a vertical blanking period ([0010] AAPA).

11. In regards to claim 14, AAPA teaches the display device according to claim 10, wherein said gradation data is video data [0002-0010].

12. In regards to claim 15, AAPA teaches the display device according to claim 7, wherein said amplitude of the output data is changed from said second voltage range to said first voltage range, resultant gradation data being said output data at said first voltage range [0007-0011] (fig. 2 B-C).

13. In regards to claim 16, AAPA teaches the display device according to claim 15, wherein said resultant gradation includes said output data that has been latched on a rising edge of a sampling pulse [0007-0011] (fig. 2 td1 and fig. 3).

14. In regards to claim 17, AAPA teaches the display device according to claim 16, wherein said resultant gradation includes said output data that has been latched on a falling edge of a sampling pulse (fig. 3 (a) and falling edge).

15. In regards to claim 18, AAPA teaches the display device according to claim 15, wherein a horizontal driving circuit converts said resultant gradation data into analog signals [0006].

16. In regards to claim 19, AAPA teaches the display device according to claim 18, wherein a vertical driving circuit sequentially selects pixels through gate lines, said pixels selected through said gate lines being driven by said analog signals [0006].

17. In regards to claim 20, AAPA teaches the display device according to claim 19, wherein said pixels are arranged in a matrix form [0005].

18. In regards to claim 21, AAPA teaches the display device according to claim 7, wherein an active device for processing said resultant gradation data is formed by low-temperature polysilicon [0008].

19. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Iemoto, in view of Ochiai et. al (US 6,897,909) hereinafter, Ochiai.

20. In regards to claim 22, AAPA and Iemoto differ from the claimed invention in that AAPA and Iemoto do not disclose wherein an active device for processing said resultant gradation data is formed by continuous grain silicon.

However, Ochiai teaches a system and method wherein an active device for processing said resultant gradation data is formed by continuous grain silicon (col. 23, lines 39-52).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify AAPA and Iemoto to include the use of an active devices for processing the gradation data is formed by CGS as taught by Ochiai in order to implement smaller sized TFTs which save space and enable more light to pass through to the view for better picture quality.

(10) Response to Argument

The Examiner rejected claims 7-21 as being unpatentable over the "Background Art" of the specification for the present application (AAPA) in view of Japanese Application No. 2002-009594.

A. claims 7-11, 13-17,19-21 stand or fall together

1) In response to Applicant's remarks that AAPA and Iemoto, either individually or as a whole, fail to disclose, teach, or suggest a display device wherein output data during a quiescent period is dummy data, said output data during a period other than said quiescent period being said amplified gradation data.

a) Examiner concedes AAPA fails to teach wherein the output data during a quiescent period is dummy data.

REPLACEMENT SHEET

Fig.1
BACKGROUND ART

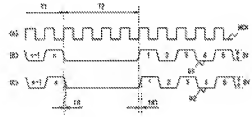

Fig.2
BACKGROUND ART

b) Iemoto, however, teaches a delay time stabilizing circuit with pulse generating means in order to reduce fluctuations associated with a delay time (abstract).

Iemoto states in the solution of the abstract, " SOLUTION: The delay time stabilizing circuit 1 of this invention is provided with a dummy pulse generating means 30 and a pulse mixer means 50 that insert a dummy pulse signal whose pulse width differs from that of a target signal into between the target signal and a target signal desirably to be delayed in order to reduce fluctuations in the operating frequency of the circuit 1." Therefore, Examiner respectfully disagrees with Applicant contentions that Iemoto fails to teach wherein output data during a quiescent period is dummy data

because dummy pulse generating means (30) outputs a dummy pulse when the present signal is not the "target signal", or quiescent period.

Applicant also contends that Iemoto fails to disclose, teach, or suggest mix-signals TD3 as including amplified gradation data. However, Examiner is relying on AAPA to teach wherein the amplified gradation data being gradation data at a second voltage range, as can be seen in fig. 2 of AAPA, (c) is outputted at 6v which is amplified from 3v.

c) Combination of AAPA and Iemoto as a whole.

Iemoto is merely relied on to teach the insertion of dummy data during a quiescent period. Examiner notes the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Under these facts, Applicant contends that Iemoto fails to teach a level shifter. However, as noted above, AAPA is relied upon to teach the level shifter (fig. 1 level shifter AAPA). Applicant also contends the Final Office Action and the Advisory Action fail to show where, how, and why the skilled artisan would have integrated the level shifter (1) of AAPA into the circuit (1) of Iemoto. Examiner asserts it is well within the skill of one of ordinary skill in the art to recognize the problems associated with delays in logic circuits, as discussed in AAPA, and look to teachings in

the art that attempted to solve the recognized problems and incorporate these teachings into the current logic gates of the current level shifter.

To summarize examiner's combination of references, AAPA is being relied upon to teach a level shifter (fig. 1 (1) AAPA), wherein the level shifter operates such that there are quiescent periods of time (See T2 fig. 2 AAPA). Iemoto is being relied upon to teach the concept of inserting dummy data during a quiescent period (Abstract Iemoto). AAPA, then, is being modified to include the concept of inserting dummy data during a quiescent period. The combination of AAPA and Iemoto would teach AAPA's quiescent period (fig. 5 T2 AAPA) having inserted within it dummy data for the benefit of providing a delay time stabilizing means that does not deteriorate timing accuracy (Abstract Iemoto).

Applicant contends the Final Office Action and the Advisory action fails to specify the element within (1) of Iemoto that the level shifter (1) of AAPA is intended to replace. But, as noted above test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Again, as noted in the preceding paragraph, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by the concepts of Iemoto.

Applicant asserts the Final Office action fails to show the alleged output data of AAPA and the alleged output data of Iemoto as being one in the same. Examiner respectfully disagrees and contends that the test is not whether the two outputs have to be one in the same. Again, as noted above, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by the concepts of Iemoto, therefore, whether or not the outputs are the same is irrelevant.

Applicant contends the Final Office Action and the Advisory action failed to specify the output within circuit (1) of Iemoto that the alleged output data of AAPA is intended to replace. But, as noted above test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Again, as noted in the preceding paragraphs, examiner is not relying on Iemoto for the replacement of components, but the level shifter of AAPA as modified by the concepts of Iemoto.

Applicant contends the Final Office Action fails to show the time for the alleged quiescent period of AAPA and the alleged quiescent period of Iemoto as being one in the same. But, as noted above the test is not whether the quiescent periods are the same but what the combined teachings would have suggested to one of ordinary skill in the art. Again, as noted in the preceding paragraphs, examiner is not relying on Iemoto

for the replacement of components, but the level shifter of AAPA as modified by the concepts of Iemoto.

In response to Applicant remarks how the skilled artisan would have considered any of the mix-signals TD3 of Iemto as including amplified gradation data. However, the examiner is relying on AAPA to teach amplified gradation data.

Applicant also contends the Final Office action fails to show where and how the output data would have been gradation data from AAPA in one instance and any of the mix-signals TD3 from Iemoto in the next instance, especially, when there is no disclosure of T2 of AAPA within Iemoto. However, examiner is not asserting output data would have been gradation data from AAPA in one instance and any of the mix-signals TD3 from Iemoto in the next instance, but the combined teachings of AAPA and Iemoto would have suggested to one of ordinary skill in the art, with respect to a level shifter, wherein output data during a quiescent period is dummy data.

B. Claim 12 Stands or falls alone.

1. Applicant contends AAPA fails to teach or suggest a display device wherein said quiescent period is a horizontal blanking period because the Office Action fails to identify a teaching or suggestion in either.

In response to Applicant's remarks the Final Office action and Advisory Action fail to show features, within claim 12 on appeal, are the same as those with AAPA. Examiner respectfully disagrees.

Fig. 3 of AAPA discloses a vertical blanking period (VBL). The corresponding section of AAPA [0010] also discuses (VBL). AAPA states," FIG. 3, in the case where each bit D1 (FIGS. 3(B1) and 3(B2)) of the gradation data is level-shifted and is latched by a subclock SCK (FIG. 3(A)) if the gradation data is data supplied at a high transfer speed, output data D2A of the level shifter 1 can be correctly latched by the subclock SCK (FIGS. 3(B1) and 3(C1)) during the period T1 in which the logical level of each bit D1 of the gradation data switches at the duty ratio of 50 (%), but immediately after a vertical blanking period VBL, for example, the output data D2 of the level shifter 1 cannot be correctly latched (FIGS. 3(B2) and 3(C2))." [0010]

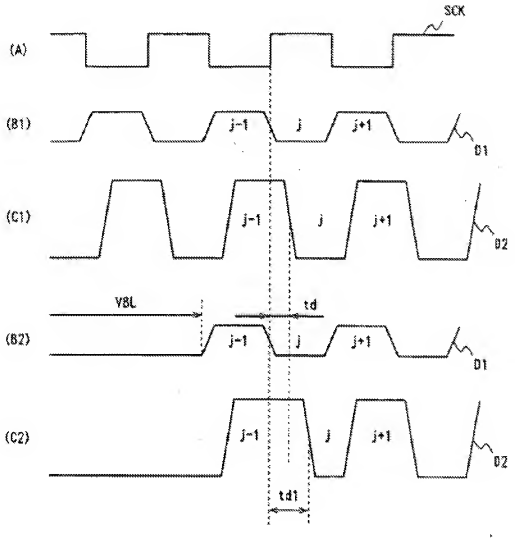

Fig.3
BACKGROUND ART

Also, with respect to fig. 2 of AAPA, AAPA mentions a quiescent period T2 but does not expressly state T2 is a "horizontal blanking period" in the background discussion. Applicant, on page 7, line 20, labels T2 as a horizontal blanking period in the Disclosure of the Invention.

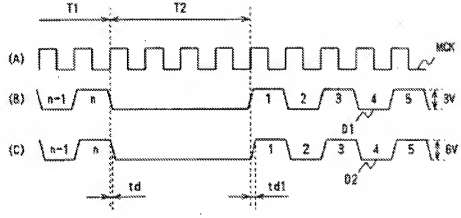

Fig.2
BACKGROUND ART

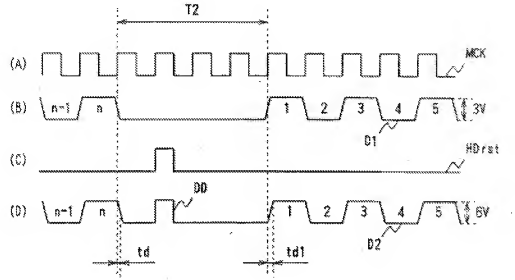

Fig.5

Therefore, Examiner asserts, while AAPA teaches a VBL [0010], whether Applicant inserts the dummy data directly into line (b), the VBL, or inserts the dummy data through line (c) (horizontal blanking period), is a matter of design choice because the function it performs is the same, namely inserting dummy data into the quiescent period. Furthermore, examiner points to page 20, line 17, wherein applicant states, "[0075] [i]n the above description of the embodiments, reference has been made to the case where dummy data is inserted at the output stage of a level shifter, but the present invention is not limited to this example. If even a variation in delay time in the level shifter becomes a problem when gradation data is to be processed at a far higher speed, dummy data may also be inserted at the input side of the level shifter." Examiner notes inserting dummy data during the horizontal period is not limited to horizontal blanking period but may also be inserted during the vertical blanking period.

C. 18 stands or falls alone.

1. Applicant asserts AAPA and Iemoto either individually or as a whole fail to disclose, teach or suggest a display device wherein a horizontal driving circuit converts said resultant gradation data into analog signals. Examiner respectfully disagrees. Gradation data applied from a horizontal driving circuit which is sequentially inputted in raster scan order to an LCD using TFTs, using a level shifter is analog data. Please see referenced Hei 10-177368 mentioned in [007] which further discusses processing of analog signals (claim 1).

II. Claim 22 Stands or fall alone.

A. AAPA and Iemoto either individually or as a whole fail to disclose, teach or suggest a display device wherein said quiescent is a horizontal blanking period. Examiner respectfully disagrees. A horizontal blanking period is not mentioned in the claim tree, therefore these arguments are moot.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Grant D Sitta/
Examiner, Art Unit 2629

Conferees:

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629